ETSVL005- 2017- A Cost and Power Efficient Image Compressor VLSI Design With Fuzzy Decision and Block Partition for Wireless Sensor Networks

Abstract

This paper presents a novel hardware-oriented image compression algorithm and its very large-scale integration (VLSI) implementation for wireless sensor networks. The proposed novel image compression algorithm consists of a fuzzy decision, block partition, digital halftoning, and block truncation coding (BTC) techniques. A novel variable-size block partition technique was used in the proposed algorithm to improve image quality and compression performance. In addition, eight different types of blocks were encoded by Huffman coding according to probability to increase the compression ratio further. In order to achieve the low-cost and low-power characteristics, a novel iteration-based BTC training module was created to get representative levels and meet the requirement of wireless sensor networks. A prediction and a modified Golomb-Rice coding modules were designed to encode the information of representative levels to achieve higher compression performance. The proposed algorithm was realized by a VLSI technique with an UMC 0.18-μm CMOS process. The synthesized gate counts and core area of this design were 6.4 k gate counts and 60 000 μm2, respectively. The operating frequency and power consumption were 100 MHz and 3.11 mW respectively. Compared with previous JPEG, JPEG-LS, and fixed-size BTC-based designs, this work reduced 20.9% gate counts more than previous designs. Moreover, the proposed design required only a one-line-buffer memory rather than a frame-buffer memory required by previous designs.

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